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D E C I S I O N
of 12 February 2004

Case Number: T 0081/03 - 3.5.1

Application Number: 91908374.1

Publication Number: 0525068

IPC: G06F 13/16, G06F 12/02, G06F 12/06, G06F 13/376

Language of the proceedings: EN

Title of invention:
Semiconductor memory device

Patentee:
Rambus Inc.

Opponents:
MICRON EUROPE Ltd et al
Infineon Technologies AG
Hynix Semiconductor Deutschland GmbH
MICRON Semiconductor Deutschland GmbH

Headword:
Semiconductor memory device/RAMBUS

Relevant legal provisions:
EPC Art. 56, 59, 114(2), 123(2) and (3), 125
EPC R. 27(1)(c)
RPBA Art. 11(6)

Keyword:
"Amendments - extension of scope of protection (no)"
"Late filed requests - admissibility (auxiliary requests 3 to 5: no)"
"Decision re appeals - remittal (no)"
"Inventive step - (main request and auxiliary request 1: no")

Decisions cited:
G 0002/88, G 0001/93, T 0249/93, T 0633/97, T 1126/97, T 1149/97

Catchword:

1. Amendments to a European patent may be based on the whole reservoir of features originally disclosed in the corresponding application provided that Article 123(3) EPC is not infringed by such amendments, due account being taken of the stipulations of Article 69(1) EPC (point 3.9 of the reasons).

2. The general, abstract concern that the addition of a feature to a claim after grant leads to an extended scope of protection as the resulting combination of features might give rise to a different evaluation of equivalents in infringement proceedings is not in itself a sufficient reason for not allowing the addition of limiting features under Article 123(3) EPC (point 3.7 of the reasons).

3. Requests raising new issues which would require a further written phase in order to be properly dealt with are to be regarded as belated even if filed at a point in time just before the minimum period set by the Board in a summons to oral proceedings (point 2.4 of the reasons).

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0081/03 - 3.5.1

DECISION
of the Technical Board of Appeal 3.5.1
of 12 February 2004

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Decision under appeal:

Interlocutory decision of the Opposition Division of the European Patent Office posted 27 November 2002 concerning maintenance of European patent No. 0525068 in amended form.

Composition of the Board:

Chairman: S. V. Steinbrener
Members: R. S. Wibergh
B. J. Schachenmann

Summary of Facts and Submissions

I. This case concerns the appeals filed against the decision of the Opposition Division finding European patent No. 0 525 068 in amended form to meet the requirements of the EPC.

II. The patent is based on patent application WO-A-91/16680. Claim 103 of this application reads:

"103. A semiconductor device capable of use in a semiconductor bus architecture including a plurality of semiconductor devices connected in parallel to a bus wherein said bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by said semiconductor device for communication with substantially every other semiconductor device connected to said bus, and has substantially fewer bus lines than the number of bits in a single address, said semiconductor device comprising
connection means adapted to connect said semiconductor device to said bus, and
at least one modifiable access-time register accessible to said bus through said connection means, whereby data may be transmitted to said register via said bus which establishes a predetermined amount of time that said semiconductor device thereafter must wait before using said bus in response to a request."

III. Claim 1 as granted reads:

"1. A semiconductor memory device having at least one memory array (1) which includes a plurality of memory cells, the memory device comprising:
clock receiver circuitry (101, 111) for receiving an external clock signal (53, 54) having a fixed frequency;
a programmable access-time register for storing a value which is representative of a number of clock cycles of the external clock signal (53, 54) to transpire after which the memory device responds to a read request; and
a plurality of output drivers (76) for outputting data onto an external bus (18, 65) in response to a read request, wherein the output drivers (76) output data on the external bus (18, 65) after the number of clock cycles of the external clock transpire and synchronously with respect to the external clock signal (53, 54)."

IV. Four oppositions were filed against the patent, based on Article 100(a), (b), (c) EPC. The Opposition Division found that the granted patent did not fulfil the requirements of Article 123(2) EPC since the original application disclosed only a multiplexed bus. The claims finally accepted by the Opposition Division on the basis of an auxiliary request contained a number of features present in claim 103 as initially filed but absent from claim 1 as granted.

V. This decision was appealed by all parties to the proceedings.

In its grounds of appeal the patent proprietor requested that the patent be upheld unamended, or, as

auxiliary requests 1 to 6, that it be maintained in accordance with one of six sets of amended claims filed with the grounds. Accelerated prosecution of the appeal was also requested.

The opponents requested revocation of the patent in its entirety. Opponent 04 also requested acceleration of the procedure. New prior art documents were filed by the opponents with the statements of grounds, in particular:

D30: D. K. Morgan, "The CVAX CMCTL - A CMOS Memory Controller Chip", Digital Technical Journal, No. 7, August 1988, pages 139 to 143.

VI. By communication dated 14 November 2003, the Board summoned the parties to oral proceedings to commence on 10 February 2004. Various general observations were made on the claims on file. The Board indicated that it might disregard evidence not submitted in good time prior to the oral proceedings. This also applied to amendments to the patent documents, which were to be filed "as early as possible (at least one month before the date set for the oral proceedings)."

VII. On 9 January 2004 the patent proprietor filed claims according to new auxiliary requests 1 to 19 and 1' to 19'. Each of the primed requests differed from the respective unprimed ones in that dependent claim 5 (against which a separate objection had been raised by the opponents) was deleted.

VIII. By letter dated 12 January 2004, opponent 02 filed two new prior art documents:

D31: Intel Application Note AP-132, "Designing Memory Systems with the 8K x 8 iRAM", June 1982, pages 3-41 to 3-45; Intel Preliminary Data Sheet "2186 - 8192x8 Bit Integrated RAM", September 1982, pages 3-281; and one undated sheet without page number relating to the 2186 family.

D32: B. Prince et al., "Semiconductor Memories", John Wiley & Sons 1983, pages 9-13, 48-53, 66, 67, 74, 75, 188-191.

IX. In the course of the oral proceedings before the Board held on 10-12 February 2004, the patent proprietor reacted to the Board's opinion that the claimed memory device had originally been disclosed only in combination with a specific bus structure by withdrawing its previous main request and all but five of the auxiliary requests filed on 9 January 2004 (and similarly for the corresponding primed requests not comprising claim 5). The claims of the remaining auxiliary requests were slightly amended and re-filed as main request and first, third, fourth and fifth auxiliary requests. The second auxiliary request was to remit the case to the Opposition Division.

X. Claim 1 according to the *main request* reads as follows:

"A Dynamic Random Access Memory (DRAM) semiconductor device having at least one memory array which includes a plurality of memory cells, the DRAM comprising: connection means adapted to connect the DRAM to an external bus which is a part of a semiconductor bus architecture, the semiconductor bus architecture

including a plurality of semiconductor devices connected in parallel to the external bus, wherein the external bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by the DRAM for communication with substantially every other semiconductor device connected to the external bus, and has substantially fewer bus lines than the number of bits in a single address;

clock receiver circuitry (101, 111) for receiving an external clock signal (53, 54) having a fixed frequency;

a programmable access-time register for storing a value which is representative of a number of clock cycles of the external clock signal (53, 54) to transpire after which the DRAM responds to a read request, the programmable access-time register being accessible to the external bus through the connection means, wherein the DRAM receives the read request synchronously with respect to the external clock signal, and wherein data may be transmitted to the programmable access-time register over the external bus to set the value in the programmable access-time register;

a plurality of output drivers (76) for outputting data onto the external bus (18, 65) in response to the read request;

wherein the output drivers (76) output data on the external bus (18, 65) after the number of clock cycles of the external clock signal transpire and synchronously with respect to the external clock signal (53, 54), so that the read request and the corresponding response are separated by the number of clock cycles as selected by the value stored in the programmable access-time register."

XI. Claim 1 according to the *first auxiliary request* reads as follows:

"A Dynamic Random Access Memory (DRAM) semiconductor device having at least one memory array which includes a plurality of memory cells, and being capable of use in a semiconductor bus architecture including a plurality of semiconductor devices connected in parallel to an external bus, wherein said external bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by the DRAM for communication with substantially every other semiconductor device connected to said external bus, and has substantially fewer bus lines than the number of bits in a single address, the DRAM comprising:
connection means adapted to connect the DRAM to said external bus;
clock receiver circuitry (101, 111) for receiving an external clock signal (53, 54) having a fixed frequency;
at least one programmable access-time register for storing a value which is representative of a number of clock cycles of the external clock signal (53, 54) to transpire after which the DRAM responds to a read request, the programmable access-time register being accessible to the external bus through the connection means, wherein data may be transmitted to the programmable access-time register over the external bus which establishes the value in the programmable access-time register;
a plurality of output drivers (76) for outputting data onto the external bus (18, 65) in response to the read request;

wherein the output drivers (76) output data on the external bus (18, 65) after the number of clock cycles of the external clock signal transpire and synchronously with respect to the external clock signal (53, 54), so that the read request and the corresponding response are separated by the number of clock cycles as selected by the value stored in the programmable access-time register."

XII. Claim 1 of the *third to fifth auxiliary requests* differs from the previous requests mainly by the addition of three features:

"wherein the value in the programmable access-time register is programmable both during and after an initialization sequence";
"wherein each output driver (76) outputs two bits of the data during a clock cycle of the external clock signal (53, 54)"; and
"wherein a portion of the memory array (1) is automatically precharged in response to the read request, without further instructions."

XIII. The opponents argued that the patent's scope of protection had been inadmissibly extended (Article 123(3) EPC) by the reinsertion of features into claim 1 (of all sets of claims) which were present in claim 103 as initially filed but had been deleted from the main claim before grant. Moreover, the claims contravened Article 123 EPC also in that some features, although present in the initial application, were not contained in the granted patent. Furthermore, the subject-matter of claim 1 (of all sets of claims) was obvious from the cited prior art.

As to the procedural issues, those claims of the set of nineteen requests filed on 9 January 2004 which opened up new issues were inadmissible. Filing them at such a late stage was not a proof of good faith. Also the patent proprietor's unexpected request at the oral proceedings for remittal to the first instance was inadmissible. Otherwise a patent proprietor could always force a delay of a decision at will by filing claims containing features not previously discussed.

XIV. The patent proprietor argued that claim 1 (of all sets of claims) complied with Article 123(2) and (3) EPC since it had been restricted by features clearly present in the application as filed. It did not matter whether or not the features were also contained in the patent specification, as demonstrated by the clear wording of Article 123(2) EPC. The invention was new and inventive. In particular, it involved the integration on a single chip of both DRAM and a memory controller, a combination which the skilled person would not have considered at the priority date. The integration was not feasible for the large memories contemplated in D30, nor would it have been regarded as advantageous since the size of the memory associated with one controller could then not have been varied.

Furthermore, the nineteen sets of amended claims filed on 9 January 2004 were admissible since they were presented within the time limit given by the Board in the summons to oral proceedings. The new features introduced in some of the requests were anyway well known to the opponents because they had already been discussed during proceedings concerning a related

European patent opposed by the same parties. Moreover, the opponents had presented the prior art documents D31 and D32 even later and indeed after the final date indicated in the summons.

XV. The patent proprietor requested that the decision under appeal be set aside and that the patent be maintained in amended form on the basis of the following requests:

- main request as submitted at the oral proceedings,
- main request' (= main request without claim 5),
- first auxiliary request as submitted at the oral proceedings,
- first auxiliary request' (= first auxiliary request without claim 5),
- second auxiliary request: remittal of the case to the first instance for further prosecution,
- third to fifth auxiliary requests as submitted at the oral proceedings,
- third to fifth auxiliary requests' (= third to fifth auxiliary requests without claim 5).

XVI. All opponents requested that the decision under appeal be set aside and the patent be revoked.

XVII. At the end of the oral proceedings the Board announced its decision.

Reasons for the Decision

1. Admissibility of the appeals

All the appeals comply with the requirements referred to in Rule 65(1) EPC and are therefore admissible.

2. *Admissibility of the patent proprietor's requests*

2.1 On 9 January 2004, one month prior to the date of the oral proceedings before the Board, the patent proprietor filed nineteen auxiliary requests (the corresponding "primed" requests 1' to 19', in which dependent claim 5 is deleted, need no separate consideration). In the course of the oral proceedings the patent proprietor withdrew all but five of these requests (cf point IX above). Of these five requests, the Board has admitted two and rejected three as inadmissible. The reasons for this decision are given below.

2.2 As a general rule, the more complex the issues raised by amendments and the later those amendments are filed, the greater the risk that the remaining time is insufficient to consider them properly. In the case T 1126/97 (not published in the OJ EPO) the deciding board stated in point 3.1.2 that for late amendments to be admissible the following conditions should be fulfilled:

(i) there should be some justification for the late filing,

(ii) the subject-matter of the new claims should not diverge considerably from the claims already filed, in particular they should not contain subject-matter which has not previously been claimed, and

(iii) the new claims should be clearly allowable in the sense that they do not introduce new objections under the EPC and overcome all outstanding objections.

Furthermore, according to decision T 633/97 (not published in OJ EPO), point 2.2, "once oral proceedings have been arranged in appeal cases, the decision to admit new evidence or requests into the procedure should hinge neither on a fixed time limit for their submission nor on their merit. It should instead be governed primarily by a general interest in the appeal proceedings being conducted in an effective manner, i.e. in dealing with as many of the issues raised by the parties as possible, while still being brought to a close within a reasonable time". Similarly, according to Article 11(6) of the Rules of Procedure of the Boards of Appeal (OJ EPO 2003,61) a case should be ready for decision at the conclusion of the oral proceedings.

2.3 Although concerned with amendments filed during the oral proceedings, decision T 1126/97 sets out criteria which appear useful also in the present case. In particular, it is pointed out that "the subject-matter of the new claims should not diverge considerably from the claims already filed". Inspection of the five sets of claims filed at the oral proceedings as main request and auxiliary requests 1 and 3 to 5 (out of the

nineteen auxiliary requests filed on 9 January 2004) reveals that the patent proprietor demanded in particular the following features not contained in claim 1 as granted to be considered:

(a) In all sets of claims: "Data may be transmitted to the programmable access-time register over the external bus to set the value in the programmable access-time register";

(b) In the main request and auxiliary requests 3 to 5: "The DRAM receives the read requests synchronously with respect to the external clock signal";

(c) In auxiliary requests 3 to 5: "The value in the programmable access-time register is programmable both during and after an initialization sequence";

(d) In auxiliary requests 3 to 5: "A portion of the memory array (1) is automatically precharged in response to the read request, without further instructions";

(e) In auxiliary requests 3 to 5: "Each output driver (76) outputs two bits of the data during a clock cycle of the external clock signal (53, 54)"; and

(f) In all requests: "So that the read request and the corresponding response are separated by the number of clock cycles as selected by the value stored in the programmable access-time register". This last amendment was made in reaction to a comment by the Board in the annex to the summons.

2.4 In claim 1 as granted a crucial feature is - as acknowledged by the patent proprietor - the programmable access-time register. Therefore, additional features serving to further define this register can be regarded as "not diverging" in the meaning of T 1126/97. With reference to the list of features in the preceding paragraph, the additional features (a), (c), (f), and possibly (b), are not diverging and could, in accordance with the given criteria, be considered.

The additional features (d) and (e), however, are unrelated to the programmable access-time register. The feature concerning the precharging has to do with the memory array, and the feature concerning the two bits per clock cycle relates to the data bus. Each feature can be termed "diverging" in the sense that it requires examination of a solution to an entirely new technical problem. In such circumstances it is of little importance whether the requests are filed during the oral proceedings or shortly prior to them since in either case the new subject-matter would have to be discussed at the hearing and neither the Board nor the other parties could be expected to deal with it without adjournment of the oral proceedings (see T 633/97, point 2.2, last paragraph). Thus, also requests filed at a point in time just before the minimum period set by the Board in a summons to oral proceedings are to be regarded as belated if they raise issues which would require a further written phase in order to be properly dealt with.

2.5 Additionally, the opponents have pointed out that the new claim features (d) and (e) do not correspond exactly to the passages which are said to provide support for them (claim 17 as granted and paragraphs [38],[88] of the specification, respectively). Therefore, complex issues with respect to Article 123 EPC would probably have to be discussed, contrary to the criteria established by the case law.

2.6 The patent proprietor has argued that the opponents in this case were familiar with features d) and e) since they were all parties to opposition proceedings concerning a related patent during which these features had been discussed. Therefore they were well prepared to consider all auxiliary requests.

The Board notes that, regardless of whether the opponents were familiar with all the technical issues, they did not accept that the invention according to the auxiliary requests was patentable. The divergent features would still require extensive discussions.

2.7 To sum up, the Board decided not to admit any requests which involve the technical features (d) and (e) referred to above. This applies to the final auxiliary requests 3, 4 and 5. It follows that only the claims of the patent proprietor's final main and first auxiliary requests will be examined by the Board.

The patent proprietor's main request

3. *Amendments*

3.1 Claim 1 of the main request is based on claim 103 as initially filed. Claim 103 contains several features which were deleted from the main claim before grant and are now being reintroduced. The opponents have argued that these modifications of claim 1 as granted are not allowable under Article 123(2) and (3) EPC.

3.2 The opponents' first line of argument relies on decision T 1149/97 (OJ EPO 2000, 259). The first sentence of headnote III of this decision reads:

"If, in view of Articles 84 and 69 EPC, the application documents have been adapted to amended claims before grant, thereby deleting part of the subject-matter originally disclosed in order to avoid inconsistencies in the patent specification, as a rule subject-matter deleted for this reason can neither be reinserted into the patent specification nor into the claims as granted without infringing Article 123(3) EPC...".

3.3 The argument can be summarised as follows. In the patent application as initially filed the data bus features are prominent. Also in claim 103 there are several references to the bus. At the granting stage all such references were deleted from claim 1. For example, claim 103 sets out a semiconductor device "capable of use in a semiconductor bus architecture including a plurality of semiconductor devices connected in parallel to a bus wherein said bus includes a plurality of bus lines for carrying

substantially all address, data and control information needed by said semiconductor device...", whereas claim 1 as granted instead merely mentions "an external bus". The description has been similarly changed. Thus, for example, one of the objects of the invention has been changed from "to provide devices, especially DRAMs, suitable for use with the bus architecture of the invention" (application, page 7, lines 5 to 7) into "to provide a semiconductor memory device, suitable for use with the bus architecture described in the description" (specification, paragraph [0015]). In the opponents' view, this means that - in the words of decision T 1149/97 - the application documents have been *adapted to amended claims* before grant, thereby *deleting part of the subject-matter* originally disclosed *in order to avoid inconsistencies* in the patent specification. Thus, in accordance with that decision, the deleted bus features cannot be re-inserted by virtue of Article 123(3) EPC.

3.4 The Board observes that the facts of the case dealt with in decision T 1149/97 differ from those of the present case. As can be seen from points 6.1.13 and 6.1.14 of this decision, the granted patent was restricted to a specific embodiment, and alternative embodiments were deleted from the patent specification (or described as no longer belonging to the invention) in accordance with Articles 84 and 69(1) EPC in order to avoid inconsistencies with the remaining subject-matter. After grant the claim was amended by adding features which originally related to those deleted embodiments and therefore were no longer present in the patent specification. The addition, though formally restricting the claimed subject-matter even more,

simultaneously extended the scope of protection conferred by the patent due to the fact that the claim again covered embodiments which the patent as granted as a whole had excluded. Therefore, Article 123(3) EPC was considered to be infringed, and the reinsertion of the deleted subject-matter was refused. The deciding board concluded that any substantive cut-off effects of the grant of a European patent could only be based on Article 123(3) EPC (see point 6.1.10 of the reasons).

3.5 In the present case, it is true that certain expressions have been removed from the claim and the introductory part of the specification in the course of an adaptation of the latter under Rule 27(1)(c) EPC, but the complete detailed description - including the data bus - remained unchanged in the patent. The re-insertion of the bus features does not shift the claimed subject-matter as granted to cover alternative embodiments which had to be deleted before grant for reasons of inconsistency, but only limits a (too broadly) generalised claim based on the only embodiment of the invention by features of said embodiment so as to be supported by the original disclosure. Insofar as these issues are concerned, the Board cannot see any infringement of Article 123(3) EPC. An objection of inconsistency involving an incompatible embodiment has not been raised by the opponents and would also not be logical in view of their argument that those features had in fact to be re-introduced because they were essential to the invention.

Therefore the Board holds that decision T 1149/97 is not applicable to the present case.

3.6 A second line of argument presented by the opponents is that the mere fact of adding the bus features reduces the importance of the features contained in claim 1 as granted, such as the access-time register. In the words of opponent 02, the point of gravity of the claim is shifted. During infringement proceedings a judge would be more inclined to apply equivalence considerations to such apparently unimportant features. This would effectively increase the scope of protection of the patent, in contravention of Article 123(3) EPC.

3.7 Article 69 EPC and its protocol are to be applied in proceedings before the EPO whenever it is necessary to determine the protection conferred (see eg decision G 2/88 of the Enlarged Board of Appeal, point 3.3 (OJ EPO 1990, 93)). Obviously equivalence considerations often play a prominent role in national infringement proceedings and although equivalents are not mentioned in the EPC at present they will be in the protocol to Article 69 of the revised Convention EPC 2000 (see the Special Edition No. 1 of the OJ 2003, page 73). Nevertheless, in spite of the undisputable importance of the concept of equivalence for the determination of the scope of protection, if the opponents were right in their allegations it would *never* be possible to amend a claim during opposition proceedings - although provided for in the EPC - since the addition of any new feature necessarily reduces to some extent the weight of the features in the claim as granted. This is particularly true when the subject-matter of the granted claim is not new, a case in which amendments are most called for. For this reason the argument cannot be accepted. The Board thus finds that the general, abstract concern that the addition of a feature to a claim after grant

leads to an extended scope of protection as the resulting combination of features might give rise to a different evaluation of equivalents in infringement proceedings is not in itself a sufficient reason for not allowing the addition of limiting features under Article 123(3) EPC.

3.8 A third line of argument is based on the opponents' view that at least one of the features of claim 1 ("and has substantially fewer bus lines than the number of bits in a single address") is not present in this form anywhere in the patent specification but only in the patent application. According to the opponents, it should not be possible to claim subject-matter even if originally disclosed unless it is also contained in the granted patent. Otherwise third parties, who as a rule are not aware of the contents of the application corresponding to a published patent, would be taken by surprise. In the opponents' view the German jurisprudence tends in this direction. The principle should apply to European proceedings as well for the same reason of security for third parties, or by virtue of Article 125 EPC.

The patent proprietor, referring to Article 123(2) EPC, denies that there exists such a general bar against amendments after grant having no support in the patent specification.

3.9 The Board agrees with the patent proprietor that there is no basis in the EPC for the idea that amendments after grant must be based on subject-matter contained in the patent specification. The wording of Article 123(2) EPC is unambiguous: a European *patent*

may not be amended in such a way that it concerns subject-matter which extends beyond the content of the *application as filed*. It is Article 123(3) EPC which is intended to protect the interests of third parties, as pointed out by the Enlarged Board of Appeal in the decision G 1/93 (OJ EPO 1994, 541), point 9 of the reasons: "Article 123(3) EPC is directly aimed at protecting the interests of third parties by prohibiting any broadening of the claims of a granted patent, even if there should be a basis for such broadening in the application as filed". In the second half-sentence of this quotation the Enlarged Board in fact implicitly refers to Article 123(2) EPC.

As discussed before, decision T 1149/97 also does not advocate a general cut-off effect in this connection unless Article 123(3) EPC is infringed.

Finally, Article 125 EPC can hardly be invoked in this context because it concerns "principles of procedural law" to be taken into account only in "the absence of procedural provisions in this Convention". It is questionable whether amendments to a European patent are a matter of procedural law, and in any case the Convention contains provisions in this respect.

It follows that amendments to a European patent may be based on the whole reservoir of features originally disclosed in the corresponding application provided that Article 123(3) EPC is not infringed by such amendments, due account being taken of the stipulations of Article 69(1) EPC. Moreover, the Board observers that this view is shared in the literature (see B. Günzel: "Materielle Zäsurwirkung der Patenterteilung

gemäß dem Europäischen Patentübereinkommen - Eine neue 'Falle' für den Patentinhaber?", GRUR 2001, Heft 10-11, pages 932 to 937).

3.10 Since no further objections have been raised against the amendments made, the Board is satisfied that the provisions of Article 123 EPC are not contravened.

4. *Construction of claim 1*

4.1 The patent proprietor argued at the oral proceedings that the feature stating that "the external bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by the DRAM for communication with substantially every other semiconductor device connected to the external bus" merely means that the bus is capable of transmitting this information. It does not necessarily imply that *the same* bus lines carry all three different kinds of information (i.e. that the bus is "multiplexed").

4.2 The feature in question is based on claim 103 of the patent application as originally filed. In the Board's view the wording of the feature taken in isolation is ambiguous. It seems however that its meaning can be deduced from the application as a whole. First, the description contains no example of a non-multiplexed bus. Second, and more importantly, a similarly phrased passage in the description - "The bus carries substantially all address, data and control information needed by devices for communication with other devices on the bus" (page 11, lines 23 to 25) - clearly refers to a "multiplexed" bus (page 11, line 17), on which

"address and data information can be sent over the same lines" (page 12, line 6). Against this background it appears less relevant that, as pointed out by the patent proprietor, claim 103 as originally filed does not contain the word "multiplexed". Thus the Board is of the opinion that the only interpretation of the feature which is supported by the application as a whole is that the bus is multiplexed.

4.3 The invention as claimed is a "Dynamic Random Access Memory (DRAM) semiconductor device". It has been discussed during the opposition proceedings whether the expression "semiconductor device" necessarily implies a single chip or whether it also refers to devices made up of a plurality of chips, for example separate ones for the controller and the memory arrays.

It appears from the available prior art that in this technical field the word "device" is indeed used in the meaning of "single chip". In D31, for example, it is first said that an "iRAM is an entire dynamic RAM system integrated onto a *single silicon chip*, including the memory array, refresh logic, arbitration, and control logic" (pages 3 to 41, right-hand column; italics added), and later on that an "iRAM integrates all the components of a dynamic RAM memory system into a single *device*" (pages 3 to 42, right-hand column; italics added). This meaning of "device" is also supported by the description of the embodiment in the patent-in-suit. The claimed DRAM semiconductor device is therefore regarded as limited to a single IC chip, excluding a plurality of connected chips.

5. *Novelty*

5.1 The Board finds that document D30 describes the closest prior art. D30 shows in Figure 1 a "CMCTL" (CVAX Memory Controller) used as an interface between a synchronous CVAX bus, having a data width of 32 bits, and an asynchronous "private memory interconnect" (PMI). The opponents have concluded from the description of D30 that the CVAX bus is of the multiplexed type, a conclusion which the patent proprietor has not denied. The PMI connects the CMCTL to up to four memory modules, each of which consisting of up to four banks of DRAM (page 142, top). The CMCTL is implemented in a single chip (page 140, right-hand column) and may work as a synchronous slave on the bus (page 140, left-hand column), implying that it has clock circuitry. It contains a programmable (control) register used for storing a value which is representative of a number of clock cycles to transpire after which the CMCTL responds to a read request (page 143, "Registers"; page 142, right-hand column; Table 2). From Figure 1 it is clear that this value can only be transmitted over the CVAX bus. In order to output data on the bus the CMCTL must be equipped with connection means adapted to connect it with the bus, and with output drivers. The output is in synchronism with the clock since the CMCTL is said to work synchronously. Judging from Table 2 referred to above, the read request and the corresponding response are separated by the number of clock cycles as selected by the value stored in the programmable control register.

5.2 Comparing the invention as defined in claim 1 with this prior art, it can be seen that it differs from D30 in that:

- it is a DRAM semiconductor device in the meaning explained above (cf point 3.3), i.e. the memory cells and all other circuits including the register are integrated on a single chip, and

- the bus has substantially fewer bus lines than the number of bits in a single address.

Although the second difference concerns the bus to which the device may be connected rather than the device itself, there is agreement among the parties that the bus characteristics will influence the properties of the device.

5.3 Thus, the invention is new (Article 54 EPC).

6. *Inventive step*

6.1 In the Board's view, the technical effects of the distinguishing features mentioned above are not linked. Hence, the features must be considered separately. Starting with the second difference, if a bus has fewer bus lines than there are bits in the addresses, the addresses must be multiplexed (meaning that address data are split up and sent consecutively). Reducing the number of bus lines by address multiplexing is a well established technique, mentioned for instance in D32 ("At this point (1972/73) the idea of multiplexed addressing was introduced and generally accepted", see page 50) as well as in the patent-in-suit (paragraph

[0004]). Even if address multiplexing might in many cases be pointless when the bus has as many as 32 lines (the number mentioned in D30, cf page 140, left-hand column) there would be nothing surprising or unexpected about using it also for a bus of this size. On the contrary, if the skilled person had contemplated a very large memory, so that 32 address bits would not suffice, address multiplexing was an obvious solution. Whether or not such a memory would have been of any commercial value at the time is not a technical consideration and irrelevant for the question of inventive step.

6.2 As to the first difference above, the patent proprietor has argued that it was not obvious to integrate the CMCTL and the memory modules on one chip. This was not technically feasible at the priority date, as evidenced by the fact that D30 described it as difficult even to implement just the CMCTL on a single chip (cf page 140, right-hand column). Nor was higher integration desirable since it was advantageous to be able to choose freely the amount of DRAM to be used with each controller.

6.3 The Board is not convinced by these reasons. There has always been a strong tendency towards higher integration levels. For example, it was no doubt obvious to combine the four memory modules shown in Figure 1 of D30 on a single chip. It may however be less clear if the skilled person would also have included the memory controller CMCTL on such a memory chip since, as the patent proprietor has argued, the amount of DRAM is then fixed.

6.4 On this point, the opponents have referred to D31. Since the patent proprietor has objected to the admission of this document, it should first be examined whether or not the Board should disregard it under Article 114(2) EPC.

In the annex to the summons to oral proceedings the Board indicated a one-month limit in advance of the date of oral proceedings for submitting new prior art or filing new claims. This means that any such documents should have been filed on 12 January 2004 at the latest (when computed in accordance with Rule 85(1) EPC). D31 was filed on the following day.

The indication in the annex to the summons is however not a time limit in the meaning of the EPC. The Board can always exercise a certain discretion to admit documents. Naturally the time of submission is important, but so are the form and contents of the document. D31 is only a few pages long and technically not complex. Its filing was in reply to an issue raised by the Board in the annex to the summons, namely whether the expression "a semiconductor memory device" in claim 1 covered separate chips. In other words, D31 does not raise new issues (i.e. is not "diverging" in the sense of opening up a fresh case) but serves to focus the discussion on a particular issue taken up by the Board. In any case, there was sufficient time left for all parties to study it. This has not been contested by the patent proprietor. In these circumstances, the Board finds that the slight lateness is of no importance, and D31 should be admitted into the proceedings.

The same applies to document D32, submitted on the same day.

6.5 D31 concerns an "iRAM", i.e. integrated RAM. An iRAM is "an entire dynamic RAM system integrated onto a single silicon chip, including the memory array, refresh logic, arbitration, and control logic" (pages 3 to 41, right-hand column). On pages 3 to 42 there is a discussion as to whether the memory controller should be integrated within the CPU or into the memory and the latter choice is found preferable. D31 therefore appears to confirm the general tendency towards higher levels of integration also in the area of memory control.

The patent proprietor has pointed out that D31 does not recommend the use of iRAMs under all circumstances. In the last paragraph of pages 3 to 42 it is said that iRAMs "are primarily intended for use in microprocessor memories usually less than or approximately equal to 64 Kbytes, while standard DRAMs with a separate controller are more cost effective in larger memories". Thus, if it is assumed for the sake of argument that D30 concerns a large memory, D31 could be said to point away from the invention. However, cost-effectiveness is not a technical consideration. An invention may well be obvious to the technically skilled person even if, at the priority date, it does not make perfect economic sense.

The Board therefore finds that the patent proprietor has not been able to demonstrate convincingly that the skilled person would have resisted the general trend towards higher integration and would not have combined the CMCTL and the DRAM described in D30 on a single

chip. Thus, this difference is not regarded as inventive.

6.6 Another argument brought forward by the patent proprietor is that at the time the invention was made DRAMs were not synchronous devices, but asynchronous. The Board notes that regardless of whether or not this is correct, in D30, the synchronism (with respect to the bus) is a feature of the CMCTL, not of the DRAMs. Therefore, if the CMCTL were placed on a chip together with the memory, consistency with the teaching of D30 required it to remain synchronised to the bus.

6.7 Finally, the patent proprietor has pointed out that D30 nowhere mentions the problem to be solved by the present invention, namely to allow the bus to be used in intervening bus cycles for additional requests or brief bus accesses (see the patent specification, paragraph [0031]).

The Board notes that the DRAM semiconductor device of claim 1 is not involved in the bus control, which is performed by the masters. In the words of the patent-in-suit (paragraph [0039]), "the slaves never worry about arbitrating for the bus". Therefore, the DRAM device cannot be defined by the way the bus is controlled, and indeed claim 1 contains no such features. It follows that it is irrelevant that neither D30 nor D31 disclose the kind of bus control mentioned in the description of the patent-in-suit.

6.8 For these reasons the subject-matter of claim 1 does not involve an inventive step (Article 56 EPC) and the patent proprietor's main request is refused.

The patent proprietor's main request'

7. This request, differing from the main request only in the deletion of claim 5, is refused for the same reasons.

The patent proprietor's auxiliary request 1

8. Compared with the main request, claim 1 of auxiliary request 1 contains alternative formulations intended to clarify some of the features. It involves no further subject-matter which might be inventive, nor has this been argued. Thus this request is also not allowable.

The patent proprietor's auxiliary request 1'

9. Again, this request is identical with the previous one except that claim 5 has been deleted. It must also be refused.

The patent proprietor's auxiliary request 2

10. As a second auxiliary request the patent proprietor demands that the case be remitted to the Opposition Division for further prosecution (cf point XV above). The Board does not however find remittal to be appropriate in the present case. As stated in T 249/93 (not published in OJ EPO), point 2.2 of the reasons:

"... whether the Board itself decides an issue, or whether it refers the matter back to the first instance for decision is within the discretion of the Board. Parties do not have a right to have each issue decided

by two instances, however late a stage the proceedings have reached".

The patent in that case had six years to expiry, the patent-in-suit about a year and a half more. Furthermore, besides the age of the patent-in-suit it should be considered that infringement proceedings have been stayed in France and Germany in order to await the outcome of this case. Clearly, in such a situation it will be in the interest of all parties to the proceedings as well as the public that the matter be decided as quickly as possible (and indeed the patent proprietor and one opponent have requested accelerated prosecution of the procedure). Especially in such circumstances it can be expected of a patent proprietor to contribute to a speedy conclusion by using "converging" claim features (cf point 2.4 above) if the patent is amended. The opponents have argued that a patent proprietor who seeks to enforce the continuation of the opposition proceedings by filing a large number of new requests at a late stage of the appeal proceedings does not act in good faith. Although the Board does not consider that the proprietor of the patent in suit has abused the procedure, it appears that under the present circumstances a remittal of the case, resulting in the scope of the patent remaining undefined for several more years, would cause undue detriment to third parties.

Thus, the Board refuses this request.

The patent proprietor's auxiliary requests 3 to 5 and 3' to 5'

11. As already indicated (cf point 2.7), these requests are rejected as inadmissible.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The patent is revoked.

The Registrar: The Chairman:

M. Kiehl S. V. Steinbrener